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IMPLEMENTATION ON REDUCTION LUT MEMORY SIZE IN CHIRP SIGNAL GENERATION FOR SATELLITE ON-BOARD SAR

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Abstract

The synthetic aperture radar(SAR) is an active sensor that is mounted on moving platform such as aircraft or satellite. It uses electromagnetic waves for the target detecting signal which can penetrate the Earth atmosphere. For that reason, it can obtain target images regardless of the weather condition. Generally, it obtains higher resolution images with the wide bandwidth reference signal. So it takes linearly frequency modulated (LFM) signal called chirp. The instantaneous frequency of chirp signal increases as time, so that this signal can enlarge the bandwidth. In this paper, we suggest the parallel direct digital synthesizer (PDDS) chirp signal generator to generate the wide bandwidth chirp signal. The proposed PDDS signal generator consists of 4-DDS in paralleled and 4 look-up tables (LUTs) those are cascaded to each DDS unit. By using the PDDS method, it takes an advantage on the clock frequency resource, but it occupies large memory resources. When implementing SAR system in satellite platform, the size of memory unit is a critical unit.

To solve this problem, we suggest the LUT memory reduction method for using micro satellite use. Using the sinusoid, we divide one period of the sinusoid in quarter. We add an algorithm that represents a one period signal using the quarter signal of sinusoid, generate chirp signal and coded. The memory size of chirp signal generation algorithm is compared with conventional method through simulation. The memory that is used by generating chirp signal in entire system is confirmed by simulation that reduce about a quarter of conventional method. Because it applies the same algorithm in system generator, if it uses higher LUT output bit, ratio of the memory reduction will be increase. Therefore, it is considered that if it uses the same amount of memories, it would be able to design a chirp signal that has a better characteristic.

Keywords

SAR, PDDS, LUT, memory reduction , system generator,

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1. Introduction

At memory-map based chirp signal generation used in the existing satellite SAR, the memory device has the disadvantage that likely to be damaged in a space environment. Chirp signal generator of DDS method has an advantage that a low dependence on the memory device. But, there is a disadvantage that the memory consumption is large due to LUT. Chirp signal generator of conventional DDS method, it save and use all of the sine wave 1 cycle in LUT in order to represent the sine and cosine wave. In this paper, rather than 1-cycle of the sine wave stored on LUT, we propose a way to reduce the LUT memory size that is used to save only a quarter period.

2. Chirp signal generation of PDDS method

Chirp signal, as the type of linear frequency modulation(LFM) signal that frequency varies linearly with time, it's characterized with wide bandwidth. Resolution(r) of the SAR, as in Equation (1), is inversely proportional to the bandwidth of the transmitted signal, mainly use a chirp signal with a wide bandwidth in the SAR. In Equation (1), c is the speed of light, B is the bandwidth.

$$r = \frac{c}{2B} \tag{1}$$

$$s(t) = rect(\frac{t}{T}) \mathrm{A} e^{i\pi Kt^2} \tag{2}$$

Equation (2) shows a formula that defines the chirp signal, t is time, T is the pulse width, K is the chirp rate that rate of change of the frequency as time, A is the amplitude of the signal[1][2].

Although you can generate the Chirp signal using the DDS system, it requires a high clock frequency. However, in a satellite environment, it is difficult to generate the high clock frequency on the performance limits of the clock generator. Thus, by connecting a number of DDS that is relatively low operating clock in parallel, it can be used up system operation clock of the PDDS method[3].

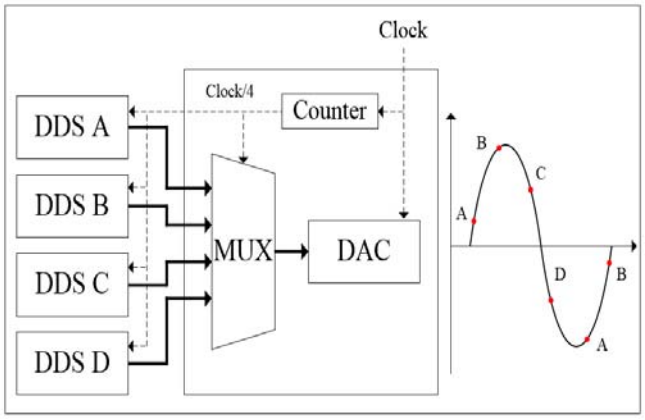

Figure 1. Structure of the PDDS.

Fig.1 is a diagram showing a PDDS method used by connecting 4-DDS blocks generating a chirp signal in parallel to the MUX. PDDS method, because 4-DDS blocks of

each generate a chirp signal, occupied more memory size in the entire system than DDS method that using 1-LUT. Chirp signal generation of PDDS method have a large proportion of LUT. If there is a large bit number of the desired output signal, it can't input a code into the board caused by the memory limit of FPGA that is hardware for signal generation. For the reason, it can be a problem of lowering the requirements of the chirp signal.

3. LUT reduction solution

In general, the phase information that necessary for the chirp signal generation is stored in a sine wave form of 1-cycle in the LUT in each PDDS block[4]. The output bit number of sine wave is taken as n, the size of the data stored in the LUT is proportional to the length of the sine wave stored in LUT and 2^n. It is necessary to use a sine wave of short cycle in the LUT in order to reduce the entire memory size as generating a signal of the same performance. As a solution, first, saving only a quarter period of sine wave in the LUT. Second, arranging the four wave as shown in Fig. 2(a). Third, making wave between $\pi/2$ and π, $3\pi/2$ and 2π to vertical symmetry (Fig. 2(b)). Finally, by changing the wave of between π and 2π, it is possible to sine wave representation of one period as shown in Fig. 2(c). In this paper, we implement digitally the chirp signal generator algorithm and the LUT reduction algorithm of PDDS method using the parameters shown in Table 1 through the system generator of the MATLAB. Then, we compare with conventional method the memory size occupied by the chirp signal generation algorithm of PDDS method using the ISE Project Navigation 14.7. Target board of ISE Project Navigation 14.7 that was used to code generation is set to Xilinx virtex-5 XC5VFX130T.

Table 1. Parameters of the signal generator used in the simulation

Parameters	Value	Unit
Pulsewidth	13.3	us
Bandwidth	75	MHz
Number of DDS	4	ea
Output bit	10	bits

Table 2. Comparison of the simulation result

	Unapplied LUT reduction	Applied LUT reduction
Number of slice LUTs (ea)	832	768
Total Memory used (KB)	432	114

Table 2 is a simulation results. As a result, in case of using the number of the LUT saved by a quarter period of the sine wave in the LUT, it was not significantly reduced from 832 to 768. However, as the used entire memory is 114 KB, it is equivalent to 26.38% of 432 KB as compared to the case of using 1-cycle.

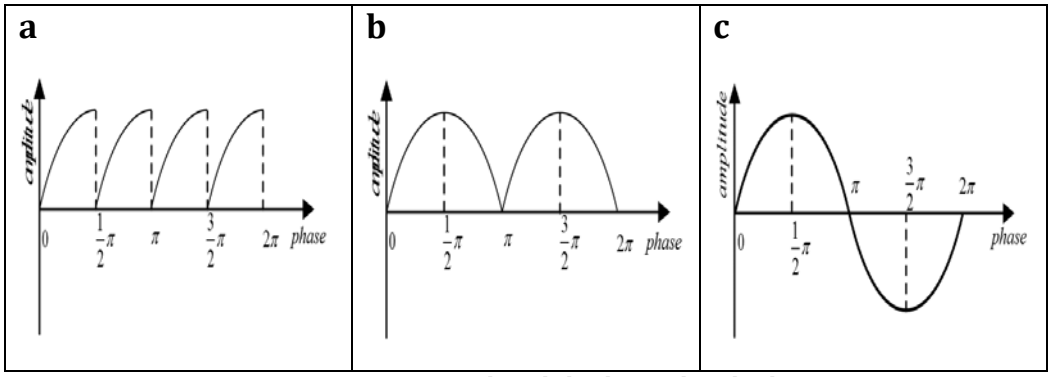

Figure 2. Sine wave representation through the phase and amplitude conversion.

4. Conclusion

In this paper, we propose on how to reduce the LUT size of the chirp signal generator mounted satellite SAR. We use the system generator that is a program to generate chirp signal and the algorithm of the PDDS method. In system generator, the period of the sine wave stored in the LUT is reduced to a quarter. We add the algorithm for representing 1-cycle by using the signal, generate a chirp signal, and coded. The memory size of chirp signal generation algorithm is compared with conventional method through simulation. The memory that is used by generating chirp signal in entire system is confirmed by simulation that reduce about a quarter of conventional method. Because it applies the same algorithm in system generator, if it uses higher LUT output bit, ratio of the memory reduction will be increase. Therefore, it is considered that if it uses the same amount of memory, it would be able to design a chirp signal that has a better characteristic.

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