Generalized Design Considerations and Analysis of Class-E Amplifier for Sinusoidal and Square Input Voltage Waveforms

Mohsen Hayati, Ali Lotfi, Marian K. Kazimierczuk, *Fellow, IEEE*, and Hiroo Sekiya, *Senior Member, IEEE*

Abstract— In this paper, analytical expressions and design equations are presented for the class-E amplifier with the MOSFET nonlinear drain-source and linear gate-drain parasitic capacitances along with the external linear shunt capacitance. The class-E amplifier characteristics are presented as functions of the ratio of the sum of the external linear shunt capacitance and the MOSFET linear gate-drain capacitance to the MOSFET drain-source junction capacitance when the switch voltage is zero. Although the effect of the MOSFET linear gate-drain capacitance is similar to that of the external linear shunt capacitance on the design of the class-E amplifier with the square input voltage, the difference between their effects should be considered for the sinusoidal input voltage, which is one of the most important suggestions in this paper. Additionally, analytical expressions of output power capability is given, which is considerable affected by the external linear shunt capacitance. Two design examples are presented with taken into account the output power as design specification at 8.7-W output power and 4-MHz operating frequency along with the PSpice-simulations and experimental waveforms.

Index Terms— External linear shunt capacitance, class-E ZVS/ZDVS conditions, output power, load resistance, nonlinear drain-to-source capacitance, linear gate-to-drain capacitance.

I. INTRODUCTION

HIGH efficiency power amplifier is a main building block in the power consumption [1]–[3]. The class-E amplifier is an efficient solution to obtain high-efficiency in various applications [4]–[7]. The shunt capacitance is the most important component in the class-E amplifier for achieving the class-E zero-voltage switching and the zero-derivative voltage switching (ZVS/ZDVS) conditions [4]–[10]. The value of the shunt capacitance is large for low frequency operation, and the

M. Hayati and A. Lotfi are with Electrical Engineering Department, Faculty of Engineering, Razi University, Tagh-E-Bostan, Kermanshah-67149, Iran (e-mail: mohsen_hayati@yahoo.com; lotfi_electrical@yahoo.com).

M. K. Kazimierczuk is with the Department of Electrical Engineering, Wright State University, Dayton, OH, 45435-0001 USA (e-mail: marian.kazimierczuk@wright.edu).

H. Sekiya is with the Graduate School of Advanced Integration Science, Chiba University, Chiba, 263-8522 Japan (e-mail: sekiya@faculty.chiba-u.jp).

MOSFET parasitic capacitance is small in total shunt capacitance that can be neglected. In this case, the external linear shunt capacitance is dominant [4]–[6]. The minimum shunt capacitance is the parasitic capacitance of the MOSFET, which depends on the MOSFET type. In addition, it is necessary to consider not only drain-source nonlinear capacitance [9]–[11] but also gate-drain linear capacitance [12]–[15] as the MOSFET parasitic capacitances. The required total shunt capacitance is uniquely determined when the operating frequency, dc-supply voltage, and output power are specified [14]. In other words, one of three specifications cannot be given if the shunt capacitance value is fixed. Therefore, it is very useful that the shunt capacitance value can be adjusted by adding the external linear shunt capacitance to the MOSFET in parallel form.

The nonlinear effect of the MOSFET drain-source capacitance increases as the operating frequency increases. The analyses of the class-E amplifier with the MOSFET nonlinear drain-source parasitic capacitance and the external linear shunt capacitance were presented in [10]. In this paper, however, the effect of the MOSFET gate-drain parasitic capacitance was ignored, which yields the switch-voltage waveform errors [14]. Therefore, both the MOSFET gate-drain and drain-source capacitances should be considered at high frequencies [12]–[17], and it is quite difficult to estimate the linear shunt capacitance.

The analysis of the class-E amplifier with the MOSFET nonlinear drain-source and linear gate-drain parasitic capacitances for both sinusoidal and square input voltage waveforms were carried out [14]. However, the load-resistance or the output power cannot be specified because the shunt-capacitance values should be fixed in these analyses. This is because that no external shunt capacitance is considered, and it is impossible to adjust the shunt capacitance values against the load-resistance or output power. This problem can be solved by designing the MOSFET with the required output parasitic capacitance value, which is not an easy task. Furthermore, under these assumptions, it is impossible to satisfy the specified load-resistance or output power and the class-E ZVS/ZDVS conditions simultaneously. Therefore, adding the external linear shunt capacitance to the MOSFET in the parallel form is an efficient and appropriate solution. In practical designs, it is required to specify the load resistance or

output power as a design specification for the class-E amplifier designs in various applications such as high-frequency electric process heating [18], DC-DC converters [19]–[26], and many power-electronics amplifiers [27]–[33].

Using the design method proposed in [34], it is possible to design of the class-E amplifier with the MOSFET linear gate-drain and nonlinear drain-source capacitances and the external linear shunt capacitance. The design approach in [34] is completely numerical design. Therefore, it is hard for many designers to use these numerical programs. In addition, with the design procedure in [34], all the design values are obtained simultaneously and directly. It is difficult to comprehend the relationships among the design specifications and element values. In this design approach, it is impossible to satisfy the specified load-resistance or output power and the class-E ZVS/ZDVS conditions simultaneously. The analytical expressions are valuable and useful, because they give the intuitive understanding of the circuit characteristics and mathematical information for designers, which cannot be obtained from circuit simulators and numerical approaches in [34].

The analytical expressions presented in this paper are valid for both the sinusoidal gate-source voltage and the square gate-source voltage, because the class-E amplifier is often driven by a sinusoidal signal in RF applications. As a result, when the dc-supply voltage and the output power or load-resistance are given as design specifications, analytical design equations show that the series-resonant-circuit elements and the external linear shunt capacitance are quite dependent on the input signal, which is one of the most important suggestions in this paper. This is because the gate-drain capacitance effect depends on the input voltage waveform. Actually, the big differences between the element values for the sinusoidal-waveform input and those for square-waveform input highlight the importance and impact of the proposed analysis. The analytical predictions agreed with the PSpice simulation and experimental results quantitatively, which proved the validity of the analytical expressions given in this paper.

II. CIRCUIT DESCRIPTION AND PRINCIPLE OPERATION

The ideal circuit topology of the class-E amplifier is shown in Fig. 1, which is composed of dc-supply voltage source V_{DD}, MOSFET as the switching element S, dc-feed inductor L_{RFC}, external shunt capacitance C_e, and series resonant filter L-C-R. The class-E switching conditions mean that both the switch voltage and the derivative of the switch voltage are zero at the switch turn-on instant, which are given by

$$v_s(\pi) = 0, \tag{1}$$

and

$$\left.\frac{dv_s}{d\theta}\right|_{\theta=\pi} = 0, \tag{2}$$
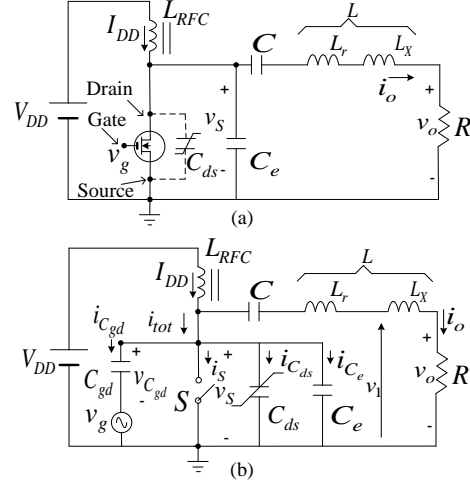
respectively.

Fig. 1. The class-E amplifier. (a) Basic circuit topology. (b) Idealized equivalent circuit.
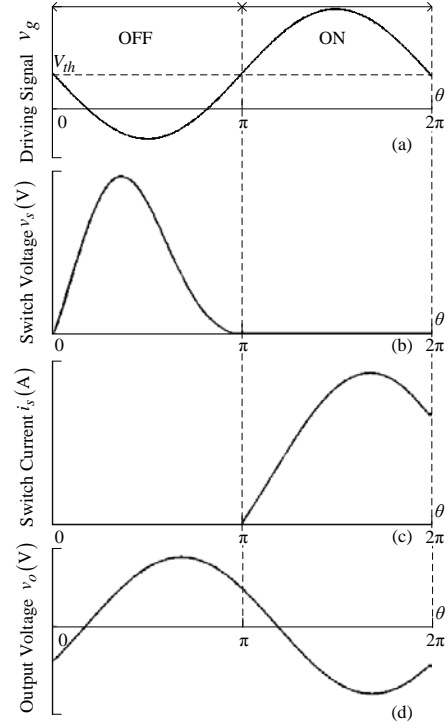

Fig. 2. Nominal waveforms of the class-E amplifier. (a) Gate-source driving voltage waveform. (b) Drain-source voltage waveform. (c) Drain-source current waveform. (d) Output voltage.

The MOSFET drain-source nonlinear parasitic junction capacitance with a nonlinear function is expressed as

$$C_{ds} = \frac{C_{j0}}{\left(1 + \dfrac{v_s}{V_{bi}}\right)^m}, \tag{3}$$

where V_{bi} is the built-in potential, which typical value is in the region from 0.5 to 0.9 V for silicon MOSFETs, v_s is the voltage between the drain and source, C_{j0} is the junction

capacitance at $v_s = 0$, and m is the grading coefficient, which is typically selected as 0.5. Fig. 2 shows the nominal waveforms of the class-E power amplifier when the switch-off duty ratio is 0.5, where V_{th} is the bias voltage of the input signal, which is the same as the threshold voltage of the MOSFET.

A. Circuit Description

The analysis in this paper is based on the following assumptions.

1) The shunt capacitance consists of the parasitic capacitances of the MOSFET and the external linear shunt capacitance C_e. The MOSFET parasitic capacitances are composed of the linear gate-drain capacitance C_{gd} and the nonlinear drain-source capacitance C_{ds} for $m=0.5$, which is expressed by (3).

2) The MOSFET is modeled as an ideal switching device with the parasitic capacitances. Namely, the MOSFET has infinite off-state resistance, zero on-state resistance, and zero switching time.

3) The input voltage across the MOSFET gate-source is expressed by

$$v_g(\theta) = -V_g \sin(\theta) + V_{th}, \tag{4}$$

where $\theta = \omega t = 2\pi ft$, f is the operating frequency, V_g is the amplitude of input signal $v_g(\theta)$, and V_{th} is the bias voltage of the input signal, which is the same as the threshold voltage of the MOSFET.

4) The inductance of the choke coil L_{RFC} is high enough to neglect its current ripple. Therefore, the dc-supply current is regarded as a direct current I_{DD}.

5) The resonant inductor L is divided into L_r and L_x. The resonant filter L_r–C is an ideal resonant filter for the operating frequency, which has zero impedance and yields zero phase shift at the operating frequency. The reactance of L_x is used to perform the phase shift of the resonant filter output current.

6) The quality factor of the resonant filter is defined as

$$Q = \frac{\omega L}{R}, \tag{5}$$

which is high enough to force a pure sinusoidal output current. The current through the L–C series-resonant circuit and the load resistance is sinusoidal at the operating frequency f

$$i_o(\theta) = I_m \sin(\theta + \varphi), \tag{6}$$

where φ is a phase shift between the input voltage and output one, and I_m is the amplitude of the load current.

7) The duty ratio of the switch is fixed at $D = 0.5$, the switching pattern is as given in Table I.

8) All elements including the MOSFET parasitic capacitances have no parasitic resistance.

Following the above assumptions, the equivalent circuit of the class-E power amplifier in this analysis can be obtained as shown in Fig. 1(b).

TABLE I
SWITCHING PATTERN

Switch	$0 \le \theta < \pi$	$\pi \le \theta < 2\pi$
	OFF	ON

B. Waveforms of Switch Voltage and Current

From the assumptions 4 and 6, the current through the MOSFET and the external shunt capacitance is

$$i_{tot}(\theta) = I_{DD} - I_m \sin(\theta + \varphi). \tag{7}$$

The switch current during the switch-off state, is given as

$$i_s(\theta) = 0, \qquad \text{for } 0 < \theta \le \pi. \tag{8}$$

Moreover, from assumption 3, the voltage across the MOSFET linear gate-drain capacitance is expressed by

$$v_{C_{gd}} = v_s - v_g = v_s + V_g \sin(\theta) - V_{th}, \text{ or } 0 < \theta \le \pi. \tag{9}$$

From Kirchhoff's current law, the relationship for the current is

$$i_{tot}(\theta) = i_{C_{gd}}(\theta) + i_{C_{ds}}(\theta) + i_{C_e}(\theta) + i_s(\theta)$$

$$= \omega C_{gd} \frac{dv_{C_{gd}}}{d\theta} + \omega \left(\frac{C_{j0}}{\sqrt{1 + \dfrac{v_s}{V_{bi}}}} + C_e \right) \frac{dv_s}{d\theta}$$

$$= \omega \left(C_{gd} + \frac{C_{j0}}{\sqrt{1 + \dfrac{v_s}{V_{bi}}}} + C_e \right) \frac{dv_s}{d\theta} + \omega C_{gd} V_g \frac{d\sin\theta}{d\theta}, \tag{10}$$

where $i_{C_{gd}}$, $i_{C_{ds}}$, and i_{C_e} are the current through the C_{gd}, C_{ds} and C_e, respectively. From (1) and (10), the following expression is obtained

$$\omega \int_0^{v_s} \left(C_{gd} + \frac{C_{j0}}{\sqrt{1 + \dfrac{v_s}{V_{bi}}}} + C_e \right) dv_s' + \int_0^{\theta} \omega C_{gd} V_g \cos(\theta') d\theta'$$

$$= \int_0^{\theta} i_{S,C_e}(\theta') d\theta', \qquad \text{for } 0 < \theta \le \pi. \tag{11}$$

The switch voltage for $0 < \theta \le \pi$ is obtained in the analytical form by performing the integration of (11), as

$$v_s(\theta) = \frac{2V_{bi}}{\gamma_1 + \gamma_2}\left[\frac{1}{\gamma_1 + \gamma_2} + h(\theta) - \sqrt{\left(\frac{1}{\gamma_1 + \gamma_2}\right)^2 + \frac{2h(\theta)}{\gamma_1 + \gamma_2} + 1}\right],$$

(12)

where

$$h(\theta) = \frac{I_{DD}\theta + I_m\left[\cos(\theta + \varphi) - \cos\varphi\right] - \omega C_{gd}V_g\sin\theta}{2\omega C_{j0}V_{bi}} + 1,$$

(13)

$$\gamma_1 = \frac{C_{gd}}{C_{j0}},$$

(14)

and

$$\gamma_2 = \frac{C_e}{C_{j0}}.$$

(15)

In (14) and (15), C_{j0} and C_{gd} are given as the design specifications and C_e is obtained to design of the class-E amplifier. From ZVS condition in (1) and (12), one obtains

$$h(\pi) = 1.$$

(16)

From (13) and (16), the dc-supply current is

$$I_{DD} = \frac{2I_m\cos\varphi}{\pi}.$$

(17)

Additionally, by substituting $\theta = \pi$ and (2) into (7) and (10), one obtains

$$I_{DD} + I_m\sin\varphi + \omega C_{gd}V_g = 0.$$

(18)

The dc-supply power and the output power are expressed as

$$P_I = V_{DD}I_{DD},$$

(19)

and

$$P_o = \frac{RI_m^2}{2},$$

(20)

respectively. From the assumptions 2 and 8, the power conversion efficiency is 100 %, namely,

$$\eta = \frac{P_o}{P_I} = \frac{RI_m^2}{2V_{DD}I_{DD}} = 1.$$

(21)

From (17) and (21), the ratio of the load resistance to input resistance R_I is

$$\frac{R}{R_I} = \frac{I_m R}{V_{DD}} = \frac{4\cos\varphi}{\pi}.$$

(22)

The amplitude of the output voltage is

$$V_m = RI_m = \frac{4V_{DD}\cos\varphi}{\pi}.$$

(23)

From (17) and (22), the dc-supply current is also expressed by

$$I_{DD} = \frac{8V_{DD}\cos^2\varphi}{\pi^2 R}.$$

(24)

The dc-supply voltage, which is the same as the average value of the switch voltage, namely,

$$V_{DD} = \frac{1}{2\pi}\int_0^{2\pi} v_s(\theta)d\theta$$

$$= \frac{1}{2\pi}\int_0^{\pi} \frac{2V_{bi}}{\gamma_1 + \gamma_2}\left[\frac{1}{\gamma_1 + \gamma_2} + h(\theta) - \sqrt{\left(\frac{1}{\gamma_1 + \gamma_2}\right)^2 + \frac{2h(\theta)}{\gamma_1 + \gamma_2} + 1}\right]d\theta.$$

(25)

By expanding the integration function in (25), one has

$$\frac{V_{DD}}{V_{bi}} = \frac{1}{\pi(\gamma_1 + \gamma_2)}\left\langle\left(\frac{\pi}{\gamma_1 + \gamma_2} + \pi + \frac{-4\cos\varphi\sin\varphi - 2\pi A_2}{A_1\pi}\right)\right.$$

$$-\int_0^{\pi}\left\{\left(\frac{1}{\gamma_1 + \gamma_2}\right)^2 + \frac{2}{\gamma_1 + \gamma_2}\times\right.$$

$$\left.\left[\frac{8\theta\cos^2\varphi + 4\pi\cos\varphi\left[\cos(\theta + \varphi) - \cos\varphi\right] - \pi^2 A_2\sin\theta}{2A_1\pi^2} + 1\right] + 1\right\}d\theta\left.\right\rangle,$$

(26)

where

$$A_1 = \frac{\omega C_{j0}RV_{bi}}{V_{DD}},$$

(27)

and

$$A_2 = \frac{\gamma_1\omega C_{j0}RV_g}{V_{DD}}.$$

(28)

The integration in (26) does not have an analytical solution, but it can be solved numerically. By substituting (22) and (24)

into (18), one obtains

$$\frac{8\cos^2\varphi}{\pi^2} + \frac{4\cos\varphi\sin\varphi}{\pi} + \frac{\gamma_1\omega C_{j0}RV_g}{V_{DD}} = 0. \tag{29}$$

(26) and (29) are expressed as functions of $\omega C_{j0}R$, $\gamma_1, \gamma_2, V_{DD}/V_{bi}$, V_g/V_{DD}, and φ. In these parameters, V_{bi} and γ_1 can be determined by selecting the MOSFET. Therefore, when four of ω, R, V_{DD}, V_g, and γ_2 are given as design specifications, the other parameter and the phase shift can be obtained using the Newton's method to solve (26) and (29). This approach is validated with the circuit design examples.

The expression for the square gate-source voltage is obtained by substituting $V_g/V_{DD} = 0$ in (26) [14]. Therefore, the phase shift in (29) is -0.567 rad, which is identical to the result in [10] and [14]. In this case, A_2 in (28) is zero then (26) is expressed as a function of $1/(\gamma_1 + \gamma_2)$. Consequently, the effect of the linear gate-drain capacitance and the external linear one are merged and just the sum of them should be considered for achieving the class-E ZVS/ZDVS conditions when the class-E amplifier is driven by the square waveform. Conversely, when V_g is not zero, which means sinusoidal input signal, the effects of linear gate-drain capacitance and external linear capacitance should be considered separately.

III. DISCUSSIONS AND COMPARISONS FOR MOSFETS

In this paper, two kinds of MOSFETs IRF510 and IRF540 from International Rectifier [35] are considered. These MOSFETs parameters that obtained from the PSpice MOSFET models are given in Table II.

TABLE II.
PARAMETERS OF THE MOSFETS

	$V_{bi}(V)$	$V_{th}(V)$	$C_{j0}(pF)$	$C_{gd}(pF)$	γ_1
IRF510	0.8	3.70	366.5	40.1	0.1094
IRF540	0.8	3.14	2408	419	0.1739

Fig. 3 shows φ as a function of V_{DD}/V_{bi} for fixed values of γ_2 and V_g, which is obtained by solving (26) and (29). Figs. 3(a) and (b) are obtained for IRF510 MOSFET and IRF540 MOSFET, respectively.

It is seen from Fig. 3 that φ increases as γ_2 increases for the fixed value of V_{DD}/V_{bi}, which means that the external shunt capacitance prepared one degree of the design freedom in comparison with the class-E amplifier with only MOSFET nonlinear drain-source parasitic capacitance as shunt capacitance in [14]. Additionally, φ converges to -0.567 rad for zero gate-drain capacitance and the square gate-source voltage, which are identical to results in [10] and [14].

It is seen from (29) that φ is always -0.567 rad for the square gate-source voltage, namely $V_g = 0$, regardless of the MOSFET type and the external linear shunt capacitance.
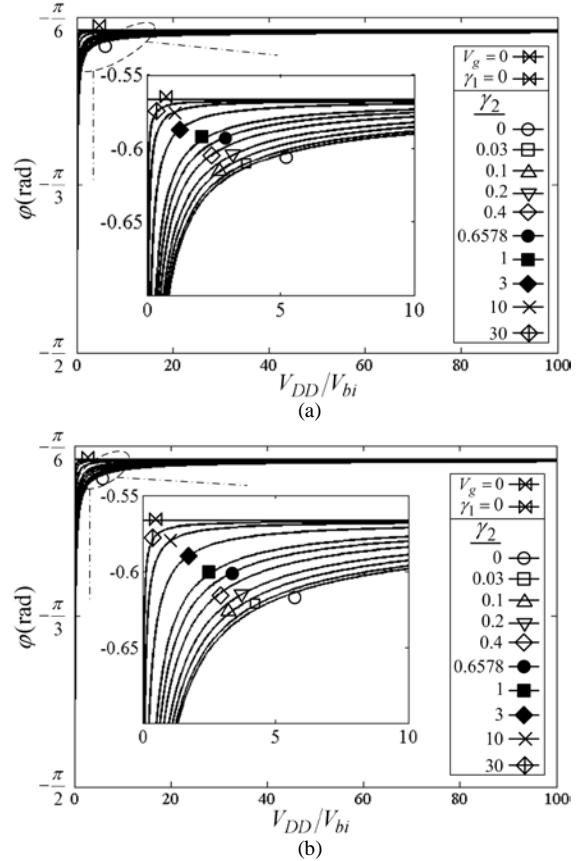

Fig. 3. φ as a function of V_{DD}/V_{bi} for fixed values of γ_2, $\gamma_1 = 0$, and $V_g = 0$. (a) The IRF510 MOSFET. (b) The IRF540 MOSFET.

Fig. 4 shows γ_2 as a function of $\omega C_{j0}R$ for $V_{DD}/V_{bi} = 25$ and the fixed values of V_g/V_{DD} and γ_1. It is seen from Fig. 4 that γ_2 increases as $\omega C_{j0}R$ decreases because the required external linear shunt capacitance increases. It is also seen that γ_2 for the square input voltage is higher than that for the sinusoidal input voltage.
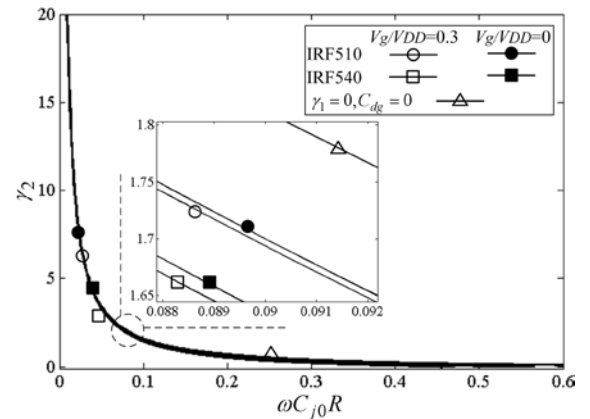

Fig. 4. γ_2 as a function of $\omega C_{j0}R$ for $V_{DD}/V_{bi} = 25$, and fixed values of γ_1 and V_g/V_{DD}.
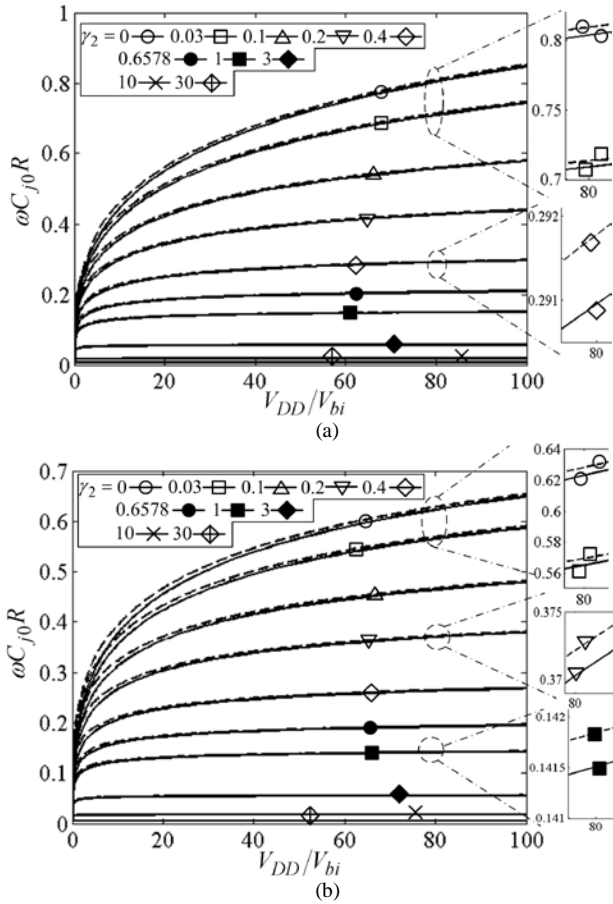
Fig. 5. $\omega C_{j0}R$ as a function of V_{DD}/V_{bi} for fixed values of γ_2, sinusoidal (solid line) and square (dash line) gate-source voltage. (a) The IRF510 MOSFET. (b) The IRF540 MOSFET.

Fig. 5 shows $\omega C_{j0}R$ as a function of V_{DD}/V_{bi} for fixed values of γ_2, and $V_g = 0$ and $V_g = 6$ V. It seen form Fig. 5 that the load resistance is determined uniquely, when γ_2 is fixed. In [14], γ_2 was equal to zero and the load-resistance cannot be given as design specification, which is the main drawback of the class-E amplifier with only the MOSFET parasitic capacitances. Therefore, the external linear shunt capacitance is regarded as an adjustment parameter to satisfy the class-E ZVS/ZDVS conditions for specified f, V_{DD}, V_{bi}, and R.

IV. VOLTAGE ACROSS RESONANT-CIRCUIT REACTANCE AND DESIGN EQUATIONS

The sum of the output voltage and the fundamental component of the voltage across the reactance L_x, which is shown in Fig. 1 (b), is expressed as

$$v_1(\theta) = V_1 \sin(\theta + \varphi_1), \tag{30}$$

where

$$V_1 = V_m \sqrt{1 + \left(\frac{\omega L_x}{R}\right)^2}, \tag{31}$$

and

$$\varphi_1 = \varphi + \arctan\left(\frac{\omega L_x}{R}\right). \tag{32}$$

From the assumption 5, the resonant filter is an ideal filter for the operating frequency. Therefore, the reactance of the series resonant filter $L_r - C$ is zero at the operating frequency. Therefore, the Fourier integral is expressed as

$$\frac{1}{\pi}\int_0^{2\pi} v_s(\theta)\cos(\theta + \varphi_1)d\theta = 0. \tag{33}$$

From (33), the analytical expression for φ_1 is given by

$$\tan\varphi_1 = \frac{\displaystyle\int_0^\pi \left[\frac{\frac{1}{\gamma_1 + \gamma_2} + h(\theta) -}{\sqrt{\left(\frac{1}{\gamma_1 + \gamma_2}\right)^2 + \frac{2h(\theta)}{\gamma_1 + \gamma_2} + 1}}\right]\cos\theta\, d\theta}{\displaystyle\int_0^\pi \left[\frac{\frac{1}{\gamma_1 + \gamma_2} + h(\theta) -}{\sqrt{\left(\frac{1}{\gamma_1 + \gamma_2}\right)^2 + \frac{2h(\theta)}{\gamma_1 + \gamma_2} + 1}}\right]\sin\theta\, d\theta}. \tag{34}$$

This expression has no analytical solution but numerical one. The value of φ_1, which is a function of $\omega C_{j0}R$, γ_1, γ_2, V_{DD}/V_{bi}, and V_g/V_{DD}, is obtained by solving (34) numerically when the design specifications are given. From (32), the reactance L_x is given as

$$L_x = \frac{R}{\omega}\tan\left(\varphi_1 - \varphi\right). \tag{35}$$

Fig. 6 shows $\omega^2 C_{j0}L_x$ as a function of γ_2 for $V_{DD}/V_{bi} = 25$ and the fixed values of V_g/V_{DD} and γ_1. It is seen that $\omega^2 C_{j0}L_x$ decreases as γ_2 increases, and it depends on the gate-source voltage waveform. $\omega^2 C_{j0}L_x$ for the square gate-source voltage is higher than that for the sinusoidal gate-source voltage. This is because the external shunt capacitance and the gate-drain parasitic capacitance have same effects, which lead to decrement of the total shunt capacitance. Moreover, $\omega^2 C_{j0}L_x$ is almost constant when γ_2 is higher than 10.
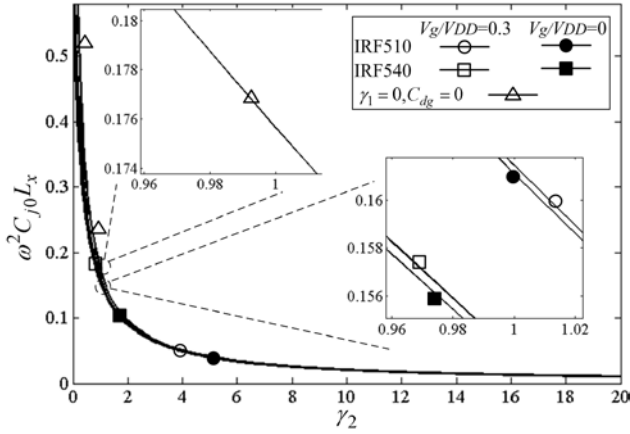
Fig. 6. $\omega^2 C_{j0} L_x$ as a function of γ_2 for $V_{DD}/V_{bi} = 25$, and fixed values of γ_1 and V_g/V_{DD}.

V. OUTPUT POWER CAPABILITY

The output power capability is defined as [10]:

$$c_p = \frac{V_{DD} I_{DD}}{|V_{s\max}| |I_{MOS,\max}|} = \frac{1}{\dfrac{|V_{s\max}|}{V_{DD}} \dfrac{|I_{MOS,\max}|}{I_{DD}}}, \tag{36}$$

where $V_{S\max}$ and $I_{MOS,\max}$ are the peak switch voltage and current, respectively. The peak switch voltage is expressed by

$$\frac{|V_{S\max}|}{V_{DD}} = \frac{|v_s(\theta)|}{V_{DD}}\bigg|_{\theta=\theta_{\max}}$$

$$= \frac{2V_{bi}}{(\gamma_1+\gamma_2)V_{DD}} \left[\frac{\dfrac{1}{\gamma_1+\gamma_2} + h(\theta_{\max}) - }{\sqrt{\left(\dfrac{1}{\gamma_1+\gamma_2}\right)^2 + \dfrac{2h(\theta_{\max})}{\gamma_1+\gamma_2}+1}} \right], \tag{37}$$

where $\theta_{\max}$ is satisfies

$$\frac{dv_s(\theta)}{d\theta}\bigg|_{\theta=\theta_{\max}} = I_{DD} - I_m \sin(\theta_{\max}+\varphi) - \omega C_{gd} V_g \cos\theta_{\max} = 0. \tag{38}$$

The peak switch current $I_{MOS,\max}$ appears during the switch on state when φ is in the range of $-\pi/2 < \varphi \le \pi/2$. It is confirmed from Fig. 3 that the range of φ satisfies this condition. Consequently, the maximum switch current is

$$I_{MOS,\max} = I_{DD} + I_m, \quad \text{for } \theta = \frac{3\pi}{2} - \varphi. \tag{39}$$

Therefore, from (22), (24) and (39), the normalized maximum switch current is

$$\frac{|I_{MOS,\max}|}{I_{DD}} = 1 + \frac{I_m}{I_{DD}} = 1 + \frac{\pi}{2\cos\varphi}. \tag{40}$$

By substituting (37) and (40) into (36), the analytical expression for the output power capability is given by

$$c_p = \frac{(\gamma_1+\gamma_2)V_{DD}\cos\varphi}{V_{bi}\left[\dfrac{\dfrac{1}{\gamma_1+\gamma_2} + h(\theta_{\max}) - }{\sqrt{\left(\dfrac{1}{\gamma_1+\gamma_2}\right)^2 + \dfrac{2h(\theta_{\max})}{\gamma_1+\gamma_2}+1}}\right] \times [2\cos\varphi+\pi]}. \tag{41}$$

Fig. 7 shows the output power capability c_p as a function of γ_2 for $V_{DD}/V_{bi} = 25$, and fixed values of V_g/V_{DD} and γ_1. It is seen from Fig. 7 that c_p for the sinusoidal gate-source voltage is lower than that for the square gate-source voltage for any value of γ_2. Also, c_p increases as γ_2 an increase, which means that the external linear shunt capacitance makes c_p to get higher. On the other hand, higher γ_1 leads to higher c_p. Therefore, including the load resistance as design specifications then obtain the required shunt capacitance is quite important to determine the output power capability, when the MOSFET is selected.

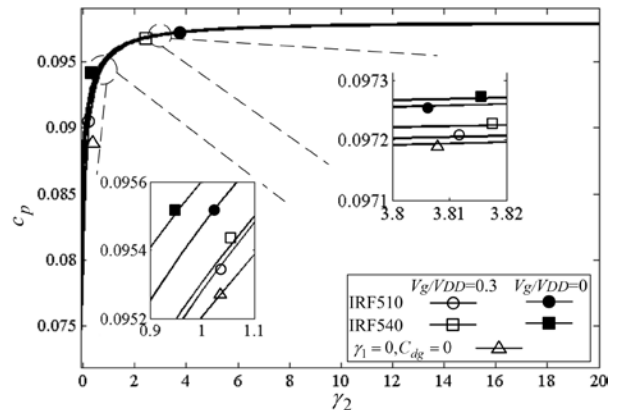Fig. 7. c_p as a function of γ_2 for $V_{DD}/V_{bi} = 25$, and fixed values of γ_1 and V_g/V_{DD}.

VI. DESIGN EXAMPLES AND DISCUSSIONS

A. Derivation of the Element Values and Design Procedure

Usually, the input parameters as design specifications for the

class-E amplifier are: operating frequency f, available dc-supply voltage V_{DD}, output power P_o or load-resistance R, loaded-quality factor Q. Moreover, the power discrete MOSFET is used as a switch device. The discrete MOSFET has fixed values of V_{bi}, C_{j0} and C_{gd}, which are design specifications when the MOSFET is selected. From these design specifications, φ and γ_2 can be obtained by simultaneously solving of (26) and (29). Therefore, it is necessary to determine the value of the external linear shunt capacitance C_e from the fixed values of C_{j0}, C_{gd}, and the load-resistance R, which are given as design specifications. The external linear shunt capacitance can be obtained from (15). Consequently, the element values are obtained from (5) and (35), which are given in section II.

B. Simulation and Measurement Procedure

The design specifications for two design examples are dc-supply voltage $V_{DD} = 20$ V, operating frequency $f = 4$ MHz, output power $P_o = 8.7$ W, and loaded quality factor $Q = 10$. The IRF510 MOSFET is selected as the switching device. The parameters of the IRF510 MOSFET can be obtained from the PSpice model provided by the manufacturer International Rectifier [35].

In this section, two design examples are given, one is for the sinusoidal gate-source voltage and the other is for the square gate-source voltage. For the sinusoidal gate-source voltage, the amplitude of the gate-source voltage is specified as $V_g = 6$ V. Therefore, $V_g/V_{DD} = 0.3$ and $\gamma_1 = 0.1094$ are given. From (22), (24), (26) and (29), $\varphi = -0.575$ rad and $\gamma_2 = 0.4321$ were also obtained. Hence, from (15) the external shunt capacitance is

$$C_e = \gamma_2 \times C_{j0} = 0.4321 \times 366.5 \times 10^{-12} = 158.37 \text{ pF.} \quad (42)$$

Therefore, from the design procedure in section II the element values are obtained as given in Table III.

TABLE III
THE VALUES OF THE ELEMENTS AND PEAK SWITCH VOLTAGE
AND CURRENT FOR THE SINUSOIDAL AND SQUARE
GATE-TO-SOURCE VOLTAGE

	Sinusoidal	Square
$R\,(\Omega)$	21.2	28.9
γ_2	0.4321	0.6639
$C_e\,(\text{pF})$	158.37	243.31
$L\,(\mu\text{H})$	8.43	11.49
$L_r\,(\mu\text{H})$	5.42	7.02
$C\,(\text{pF})$	291.8	225.5
$L_{RFC}\,(\mu\text{H})$	37.1	50.57
$V_{SM}\,(\text{V})$[1]	75.4	73.8
$I_{SM}\,(\text{A})$[2]	1.248	1.245

[1] Peak switch voltage. [2] Peak switch current.

The peak switch voltage, i.e., V_{SM} is 24.1 % lower than the breakdown drain-source voltage of IRF510 MOSFET. Therefore, it is possible to implement the class-E amplifier with the IRF510 MOSFET. The expression for the square

input-voltage waveform is obtained by substituting $V_g = 0$ [14]. Therefore, following the similar design procedure described above, it is possible to obtain the element values for the square gate-source voltage, as given in Table III. It is seen from Table III that the element values are dependent on the input signal, which means that it is quite important to consider the MOSFET linear and nonlinear parasitic capacitances for the class-E amplifier with a linear external shunt capacitance. For the second design example, the given design specifications in the first design example remained unchanged. Similar to the sinusoidal gate-source voltage design example, the peak switch voltage, and the peak switch current, for the square gate-source voltage are given in Table III, where the peak switch voltage, i.e., V_{SM} is 26.2 % lower than the breakdown drain-source voltage of the IRF510 MOSFET. Therefore, the IRF510 MOSFET is suitable for implementation of the class-E amplifier not only with the sinusoidal gate-source voltage but also with the square gate-source voltage.

Figs. 8 and 9 show the waveforms obtained from the theoretical expressions, PSpice simulations, and circuit experiments for the first and second designed class-E amplifiers, respectively. For obtaining the steady-state behaviors, long-time transient-analysis simulations are carried out for 100ns in the simulation time and the last one-period waveforms are shown as PSpice simulation waveforms for two design examples. For calculation power conversion efficiency, the measured value of the parasitic resistances, which are measured by a LCR meter of HP4284A, were used. In the experimental measurements, all the powers are measured by a digital Multimeter of 34401A.
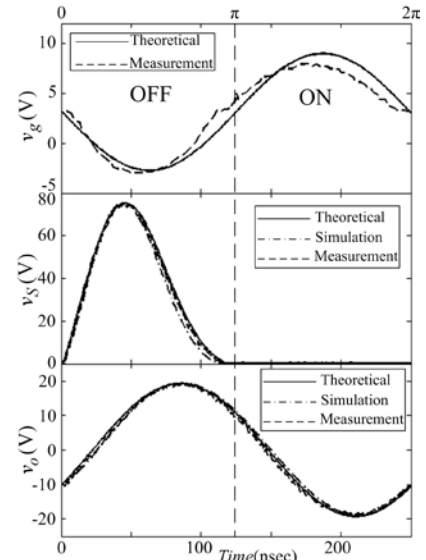

Fig. 8. Class-E power amplifier waveforms from theoretical expressions, PSpice simulations, and circuit experiment for the sinusoidal gate-to-source voltage.

The theoretical predictions, simulations and measurements results for the sinusoidal gate-to-source voltage and the square gate-to-source voltage are summarized in Table IV and V, respectively. In the first circuit design example, the experimental value of the peak switch voltage, i.e., V_{SM} is 74.9

V, and the experimental value of the output voltage amplitude V_m is 18.9 V.
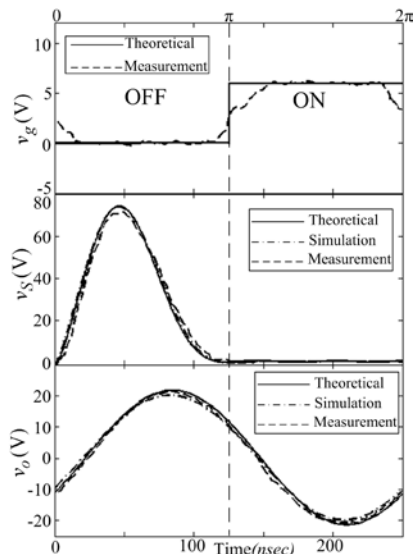

Fig. 9. Class-E power amplifier waveforms from theoretical expressions, PSpice simulations, and circuit experiment for the square gate-to-source voltage.

TABLE IV
THE THEORETICAL, SIMULATED AND MEASURED RESULTS FOR THE SINUSOIDAL GATE-TO-SOURCE VOLTAGE

	Theoretical	Simulated	Measured	Difference
V_{DD} (V)	20	20	20.0	0.00 %
f (MHz)	4	4	4.00	0.00 %
V_{SM} (V)	75.4	75.4	74.9	-0.66 %
I_{SM} (A)	1.248	1.248	1.231	-1.36 %
I_{DD} (A)	0.435	0.435	0.458	5.02 %
R (Ω)	21.2	21.2	20.9	-.1.41 %
L (µH)	8.43	8.43	8.3	-1.54 %
C (pF)	291.8	291.8	290.2	-0.54 %
C_e (pF)	158.36	158.36	157.8	-0.35 %
L_{RFC} (µH)	37.1	37.1	37.3	0.53 %
P_o (W)	8.7	8.62	8.4	-3.44 %
P_{in} (mW)	-	-	31.2	-
η (%)	93.1	91.9	91.6	-1.5 %

TABLE V
THE THEORETICAL, SIMULATED AND MEASURED RESULTS FOR THE SQUARE GATE-TO-SOURCE VOLTAGE

	Theoretical	Simulated	Measured	Difference
V_{DD} (V)	20	20	20.0	0.00 %
f (MHz)	4	4	4.00	0.00 %
V_{SM} (V)	73.8	73.8	72.4	-1.89 %
I_{SM} (A)	1.245	1.245	1.22	-2.00 %
I_{DD} (A)	0.435	0.439	0.446	2.46 %
R (Ω)	28.9	28.9	28.5	-1.38 %
L (µH)	11.4	11.4	11.3	-0.87 %
C (pF)	225.5	225.5	227.3	0.79 %
C_e (pF)	243.3	243.3	245.1	0.73 %
L_{RFC} (µH)	50.5	50.5	50.7	0.39 %
P_o (W)	8.7	8.69	8.3	-4.59 %
P_{in} (mW)	-	-	34.6	-
η (%)	93.3	92.9	92.9	-0.42 %

In the second circuit design example, the experimental value of the peak switch voltage, i.e., V_{SM} is 72.4 V, and the experimental value of the output voltage amplitude, i.e., V_m is 21.9 V. The measured efficiency for the sinusoidal gate-source voltage and the square gate-source voltage is 91.6 % and 92.9 %, respectively, at 4-MHz operating frequency. It is shown in section III that when the amount of the load-resistance decreases, the peak voltage seen at the drain decreases. Therefore, in order to obtain a specified reduced peak voltage while optimization of the efficiency at the low supply voltages, the decrement of the load-resistance and proper selection of the designed value of the dc-supply voltage is used. In two circuit design examples, the measured values of the load-network components are in good agreement with the theoretical predictions for the tested value of the load resistance.

VII. CONCLUSION

The analytical expressions for the design of the class-E amplifier with the linear and nonlinear shunt capacitances and the MOSFET linear gate-drain capacitance for satisfying the class-E ZVS/ZDVS conditions are presented. Although, for the square gate-source voltage, the effects of the MOSFET linear gate-drain capacitance and the external linear shunt capacitance are similar, for the sinusoidal gate-source voltage, their effects are considerably different, as given in the analytical expressions. This is because the gate-drain capacitance effect depends on the input voltage waveform, but the external linear capacitance effect is independent of that. Actually, the big differences between the element values for the sinusoidal-waveform input and those for square-waveform input highlight the importance and impact of the proposed analysis.

REFERENCES

[1] S.-Y. Ou, C.-Y. Tang and Z.-J. Chen, "Design and implementation of a ZCS-PWM half-bridge boost rectifier with output voltage balance control," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4646–4656, Dec. 2012.

[2] C. Branas, F. J. Azcondo, and R. Zane, "Power-mode control of multiphase resonant electronic ballast," *IEEE Trans. Ind. Electron.*, vol. 59, no.4, pp. 1770-1778, Apr. 2012.

[3] U. R. Prasanna, A. K. Rathore, "Small-signal modeling of active-clamped ZVS current-fed full-bridge isolated DC/DC converter and control system implementation using psoc," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp.1253-1261, Mar. 2014.

[4] N. O. Sokal, and A. D. Sokal, "Class E—A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 3, pp. 168–176, Jun. 1975.

[5] F. H. Raab, "Idealized operation of the class-E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CAS-24, no. 12, pp. 725–735, Dec.1977.

[6] M. K. Kazimierczuk and K. Puczko, "Exact analysis of class-E tuned power amplifier at any Q and switch duty cycle," *IEEE Trans. Circuits Syst.*, vol. CAS-34, no. 2, pp. 149–159, Feb. 1987.

[7] J. Liang, and W. Liao, "Steady-state simulations and optimization of class-E power amplifiers with extended impedance method," *IEEE Trans. Circuits Syst.-I*, vol. 58, no. 6, pp.1433–1445, June. 2011.

[8] I.-O. Lee, S.-Y. Cho and G.-W. Moon , "Three-level resonant converter with double LLC resonant tanks for high-input-voltage applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3450–3463, Sep. 2012.

[9] S.-H. Cho, C.-S. Kim and S.-K. Han , " High-efficiency and low-cost tightly regulated dual-output LLC resonant converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2982–2991, Jul. 2012.

[10] T. Suetsugu, and M. K. Kazimierczuk, "Analysis and design of class-E amplifier with shunt capacitance composed of nonlinear and linear capacitances," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 7, pp. 1261–1268, Jul. 2004.

[11] D.-Y. Kim, C.-E. Kim and G.-W. Moon, "High-efficiency slim adapter with low-profile transformer structure," *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3445–3449, Sep. 2012.

[12] D. K. Choi, and S. I. Long, "The effect of transistor feedback capacitance in class-E power amplifiers," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, no. 12, pp. 1556–1559, Dec. 2003.

[13] M. J. Chudobiak, "The use of parasitic nonlinear capacitors in class-E amplifiers," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 41, no. 12, pp. 941–944, Dec. 1994.

[14] X. Wei, H. Sekiya, S. Kuroiwa, T. Suetsugu, and M. K. Kazimierczuk, "Design of class-E amplifier with MOSFET linear gate-to-drain and nonlinear drain-to-source capacitances," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 10, pp. 2556 - 2565, Oct. 2011.

[15] M. Hayati, A. Lotfi, M. K. Kazimierczuk, and H. Sekiya, "Analysis and design of class-E power amplifier with MOSFET parasitic linear and nonlinear capacitances at any duty ratio," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5222–5232, Nov. 2013.

[16] T. Nagashima, X. Wei, T. Suetsugu, M. K. Kazimierczuk, and H. Sekiya, " Waveform equations, output power, and power conversion efficiency for class-E inverter outside nominal operation," *IEEE Trans. Ind. Electron.*, vol. 61, no. 4, pp. 1799-1810, Apr. 2014.

[17] M. K. Kazimierczuk, and X. Bui, "Class-E amplifier with an inductive impedance inverter," *IEEE Trans. Ind. Electron.*, vol. 37, no. 2, pp. 160–166, Apr. 1990.

[18] A. Sanchez-Ruiz, M. Mazuela, S. Alvarez, G .Abad, and I. Baraia, "Medium voltage–high power converter topologies comparison procedure, for a 6.6 kV drive application using 4.5 kV IGBT modules," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1462-1476, Mar. 2012.

[19] B. Zhao, Q. Yu, Z. Leng, and X. Chen, "Switched Z-source isolated bidirectional DC–DC converter and its phase-shifting shoot-through bivariate coordinated control strategy," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4657-4670, Dec. 2012.

[20] Y. Du, S. M. Lukic , B. S. Jacobson, and A. Q. Huang, "Modulation technique to reverse power flow for the isolated series resonant DC–DC converter with clamped capacitor voltage," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4617-4628, Dec. 2012.

[21] Y. C. Lin, D. Chen, Y. T. Wang, and W. H. Chang, "A novel loop gain-adjusting application using LSB tuning for digitally controlled DC–DC power converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 904-911, Feb. 2012.

[22] G. Zhou, J. Xu, and B. Bao, "Comments on predictive digital-controlled converter with peak current-mode control and leading-edge modulation ," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4851-4852, Dec. 2012.

[23] G. Zhang, Z. Li, B. Zhang, D. Qiu, W. Xiao, and W.A. Halang, "A Z-source half-bridge converter ," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1269-1279 , Mar. 2014.

[24] W. Lu, K. Zhou, D. Wang, M. Cheng, "A generic digital-order harmonic repetitive control scheme for PWM converters ," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1516-1527 , Mar. 2014.

[25] A. A. Valdez-Fernandez, P. R. Martinez-Rodriguez, G. Escobar, C.A. Limones- Pozos, and J. M. Sosa, " A model-based controller for the cascade H-bridge multilevel converter used as a shunt active filter ," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5019-5028 , Nov. 2013.

[26] L. Martinez- Salamero, G. Garcia, M. Orellana, C. Lahore, and B. Estibals, " Start-up control and voltage regulation in a boost converter under sliding-mode operation ," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4637-4649 , Oct. 2013.

[27] Z. Ouyang, O. C. Thomsen, and M. A. Andersen, " Optimal design and tradeoff analysis of planar transformer in high-power DC–DC converters ," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2800-2810, Jul. 2012.

[28] K. Rawat, and F. M. Ghannouchi, " Design methodology for dual-band Doherty power amplifier with performance enhancement using dual-Band offset lines," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4831-4842, Dec. 2012.

[29] K. Fukui, and H. Koizumi, "Class E rectifier with controlled shunt capacitor," *IEEE Trans. Power Electron*, vol. 27, no. 8, pp. 3704–3713, Aug. 2012.

[30] H. Xi, Q. Jin, and X. Ruan, "Feed-forward scheme considering bandwidth limitation of operational amplifiers for envelope tracking power supply using series-connected composite configuration," *IEEE Trans. Ind. Electron.,* vol. 60, no. 9, pp. 3915-3926 , Sep. 2013.

[31] J.-H. Chiang, B.-D. Liu, and S.-M. Chen, "A simple implementation of nonlinear-carrier control for power factor correction rectifier with variable slope ramp on field-programmable gate array," *IEEE Trans. Ind. Electron.,* vol. 9, no. 3, pp. 1322-1329 , Jul 2013.

[32] J.-C. Montano, C. Leon, A. Garcia, A. Lopez, I. Monedero, and E. Personal, "Random generation of arbitrary waveforms for emulating three-phase systems ," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4032-4040, Nov 2012.

[33] M. Hayati, A. Lotfi, M. Kazimierczuk, and H. Sekiya, "Performance study of class-E power amplifier with a shunt inductor at subnominal condition," *IEEE Trans. Power Electron*, vol. 28, no. 8, pp. 3834–3844, Aug. 2013.

[34] H. Sekiya, T. Ezawa, and Y. Tanji, "Design procedure for class-E switching circuits allowing implicit circuit equations," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3688–3696, Dec. 2008.

[35] International Rectifier [Online]. Available: http://www.irf.com/product-info/models/.

Mohsen Hayati received the BE in electronics and communication engineering from Nagarjuna University, India, in 1985, and the ME and PhD in electronics engineering from Delhi University, Delhi, India, in 1987 and 1992, respectively. He joined the Electrical Engineering Department, Razi University, Kermanshah, Iran, as an assistant professor in 1993. At present, he is an associate professor with the Electrical Engineering Department, Razi University. He has published more than 125 papers in international and domestic journals and conferences. His current research interests include a Microwave and millimeter wave devices and circuits, application of computational intelligence, artificial neural networks, fuzzy systems, neuro-fuzzy systems, electronic circuit synthesis, modeling and simulations.

Ali Lotfi received the B.Sc. degree in electrical engineering from the Iran University of Science and Technology (I.U.S.T), Tehran, Iran, in 2004, and the M.Sc. and Ph.D. degrees in electronics engineering (with Honors) from the Department of Electrical Engineering, Razi University, Kermanshah, Iran, in 2010, and 2013, respectively. His research interests are high-frequency high-efficiency power amplifiers and oscillators, RF circuits, resonant dc/dc power converters, and numerical simulation of switching circuits.

Dr. Lotfi has published more than 19 technical papers in international learned journals, 5 of them in IEEE Transactions.

Marian K. Kazimierczuk (M'91–SM'91–F'04) received the M.S., Ph.D., and D.Sci. degrees in electronics engineering from the Department of Electronics, Technical University of Warsaw, Warsaw, Poland, in 1971, 1978, and 1984, respectively.

Since 1985, he has been with the Department of Electrical Engineering, Wright State University, Dayton, OH, USA, where he is currently a Professor. His research interests are high-frequency high efficiency switching mode tuned power amplifiers, resonant and PWM dc/dc power converters, dc/ac inverters, high-frequency rectifiers, electronic ballasts, modeling and control of converters, high-frequency magnetics, and power semiconductor devices.

Hiroo Sekiya (S'97–M'01–SM'11) was born in Tokyo, Japan, on July 5, 1973. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from Keio University, Yokohama, Japan, in 1996, 1998, and 2001, respectively.

Since April 2001, he has been with Chiba University, Chiba, Japan, where he is currently an Associate Professor in the Graduate School of Advanced Integration Science. From February 2008 to February 2010, he was also with the Department of Electrical Engineering, Wright State University, Dayton, Ohio, as a visiting scholar. His research interests include high-frequency high-efficiency tuned power amplifiers, resonant dc/dc power converters, dc/ac inverters, and digital signal processing for wireless communications.

Dr. Sekiya is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan, the Information Processing Society of Japan (IPSJ), and the Research Institute of Signal Processing (RISP), Japan.