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ABSTRACT

Carrier-injection and the succeeding pre-channel-formation dynamics in organic thin-film transistor was observed using time-domain reflectometry. Having previously analyzed the depth-wise variation in the initial carrier-injection from the contact electrode to the channel region, we focus here on the succeeding pre-channel-formation dynamics. We demonstrate that a hole concentration in the semiconductor/gate insulator interface increases until its electrical capacitance is filled through contact and access resistances. Thereafter, the injected-hole distribution gradually spreads. A reduction in both contact and access resistances is crucial not only for the static characteristics of the field effect transistor but also the dynamical response.

I. INTRODUCTION

The dynamics of carrier-injection from a contact electrode into a semiconductor and the succeeding conductive channel formation in the organic thin-film transistor (OTFT) have attracted significant interest with many effective methods being extensively developed, including time-resolved electric field-induced second-harmonic generation,[1–13] charge-modulation imaging,[14–18] and others.[19] These methods have advantages in being able to optically observe carrier diffusion along the semiconductor–gate insulator interface directly. However, our method of electrical observation, time-domain reflectometry (TDR),[19] is capable of observing the thickness-wise carrier-injection, which is very important when describing the initial transient behavior of the OTFT before channel formation. Impedance spectroscopy and displacement current measurement are also the electrical impedance detection method and have been widely used in this field.[20–40] Impedance spectroscopy analyzes the device and discovers a corresponding equivalent circuit and characteristics of these components by spectroscopic method, and displacement current measurements detect variation of device impedance due to the carrier-injection and accumulation by sweeping a bias voltage. However, genuine time evolution of the device impedance was not observed in these methods because these methods are not transient but steady state measurement.

TDR is an impedance detection procedure based on the reflection of high-frequency electromagnetic wave impulses and was used, for example, in the inspection of long-distance transmission lines and in surveys of soils.[41–46] TDR detects a damaged point in a transmission line or the moisture content of the soil from the reflected electrical pulses, which include the electrical impedances of the scattering objects. In a previous study, we proposed a simple and clear technique that extends TDR in determining the transient impedance of OTFTs.[19] In this paper, we focus on pre-channel-formation phenomena between the initial vertical carrier-injection and succeeding channel formation.

II. EXPERIMENTAL DETAILS

The structure of the sample is illustrated in Fig. 1(a) and is the same as that described in a previous paper.[19] The metal–insulator–semiconductor–metal (MISM) capacitor structure corresponds to the top-contact and bottom gate thin-film transistor (TFT) structure in cross section. The MISM structure was prepared on a glass substrate by vacuum evaporation of Au for the gate electrode, by chemical vapor deposition of parylene-SR for the gate insulator

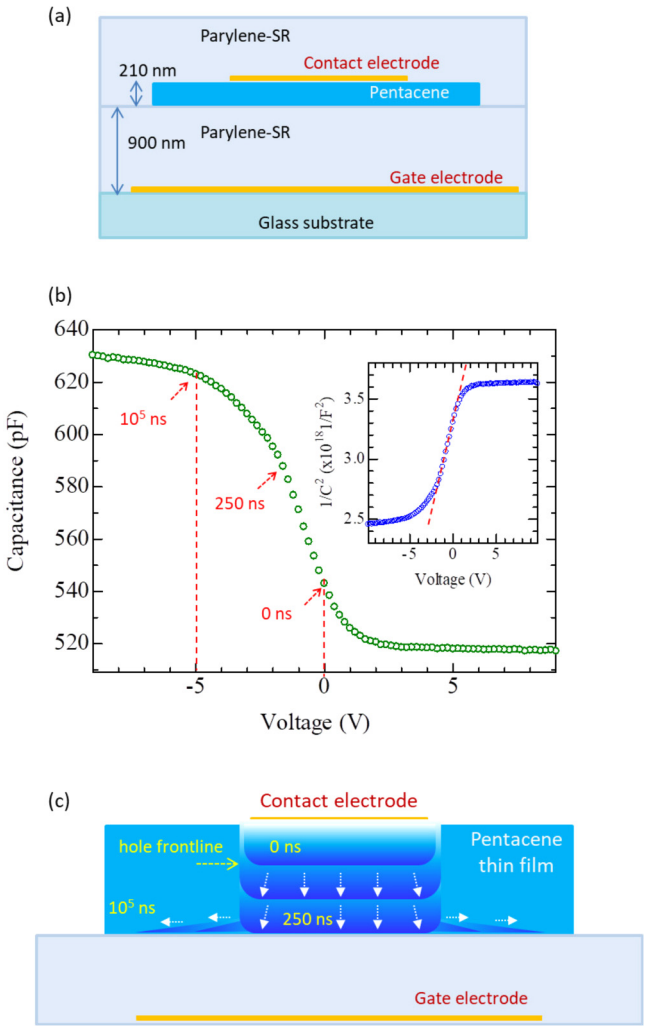

FIG. 1. (a) Illustration of the pentacene MISM sample structure. (b) Quasi-static C–V characteristics of the sample and $1/C^{1/2}$–V plot (inset). Inserted time stamps are transit times of the corresponding impedance (capacitance), which are fed back from the time-domain transmission observation (see text for details). Inset: the linear region corresponding to the progression of the front line of injected carriers. (c) Schematic illustration of the time variation of the hole distribution injected into the pentacene TFT; time stamps which correspond to that in C–V curve above are also inserted in this illustration.

layer, and by vacuum evaporation of pentacene (thickness 210 nm), and was formed on the substrate at room-temperature. The area of the pentacene thin film was $4.48 \times 4.48\,\mathrm{mm}^2$. Although the pentacene layer is thicker than that usually used in standard OTFT structures, it allows us to demonstrate vertical carrier injection clearly. We have confirmed that there is no essential difference in observed phenomena regarding the pentacene thickness. In addition, we eliminated the drain electrode in this structure to ensure an equivalent circuit employed in our analysis is simpler. The corresponding equivalent circuit of the MISM structure was similar to that used in the impedance spectroscopy of the organic light emitting diode (OLED) devices.[47,48] The area of the top-contact source electrode was $3.93 \times 3.92\,\mathrm{mm}^2$. Finally, the sample surface was passivated by a parylene-SR layer to reduce air degradation. Figure 1 shows the results of a quasi-static capacitance–voltage (C–V) measurement[49–54] of the pentacene TFT structure. The quasi-static C–V characteristics was measured under a ramp rate of $dV/dt = 2\,\mathrm{V/s}$. The gate voltage was applied to the gate electrode, and the source electrode was electrically grounded. Figure 1 shows that the sample capacitance increases with increasing negative gate voltage because of the carrier injection from the contact electrode into the organic semiconductor.[49–54] The inset of Fig. 1 is a $1/C^{1/2}$–V plot of the C–V curve. The linear region in the inset marked by a red dashed line corresponds to the bias-dependent depletion layer capacitance region, which arises with the progression of the injected-carrier front line with increasing negative gate bias. The succeeding increase in C below the negative gate bias of $-2\,\mathrm{V}$ arises from the in-plane extension of hole distribution area, i.e., the formation of a hole channel in the TFT.

The details of our technique concerning the extraction of the transient electrical impedance of the sample from the reflected or transmitted electromagnetic waves was discussed in a previous work.[19] We employed a rectangular voltage pulse wave, while simple step-pulse was used in a conventional TDR.[41–46] The rectangular-pulse wave has two edges, one rising and one falling. The rising-edge reflection includes the initial impedance of the sample if the pulse interval is sufficiently long, and the falling-edge reflection includes the transient impedance after application of the constant voltage during the gate pulse width. This fact underscores the principle of our method behind the measurement of the transient impedance during the application of the bias voltage.[19] In this work, we applied a negative $-5\,\mathrm{V}$ rectangular-pulse wave to the gate electrode to initiate hole injection from the source electrode. Although TDR treats the reflected voltage waveform, we analyzed the time-domain transmission (TDT) wave because of restrictions in the present measurement configuration. The TDT wave was acquired from the source electrode side of the MISM capacitor as done in our previous work[19] upon which this work is based.

III. RESULTS AND DISCUSSION

The TDT voltage waveforms near the falling edge (Fig. 2) were observed for various pulse widths employing a high-speed high-resolution oscilloscope. From the data, fitted curves were calculated using circuit simulator, LTspice; the equivalent circuit model was described elsewhere.[19] The baseline of the applied rectangular voltage pulse was 0 V and the pulse height was $-5\,\mathrm{V}$. Under this bias condition, the electrical impedance of the sample varies from its initial value (approximately 540 pF at 0 V in Fig. 1) to its final value (approximately 620 pF at $-5\,\mathrm{V}$ in Fig. 1) after a sufficiently long application of the bias voltage. The TDT observation with a pulse of finite width can detect the transient impedance by varying the pulse width. The TDT pulse width corresponds to the bias application time and observation of the falling edge corresponding to the detection of the transient impedance.

Each fitted curve (Fig. 2) reproduced the experimental TDT waveforms well. We confirmed that the TDT waveforms observed

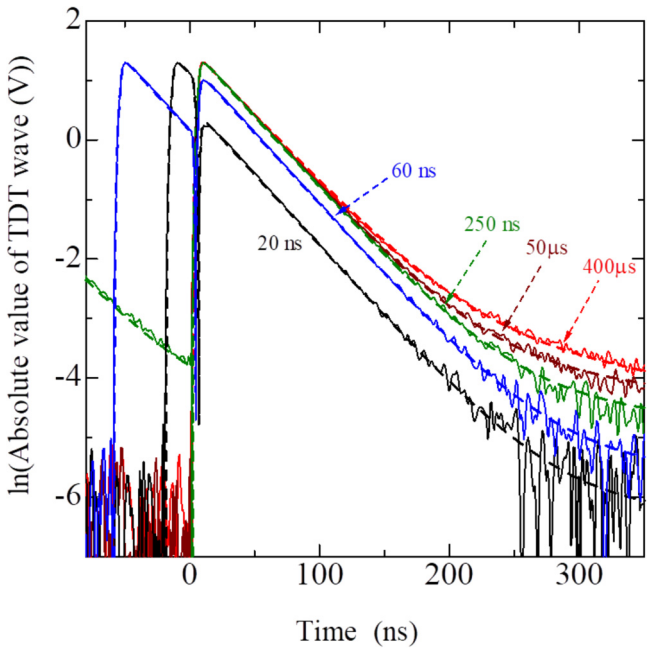

FIG. 2. Pulse width-dependent TDT waveform near the fall edge observed with a high-speed high-resolution oscilloscope. Dashed curves are fitted curves calculated using a circuit simulator.

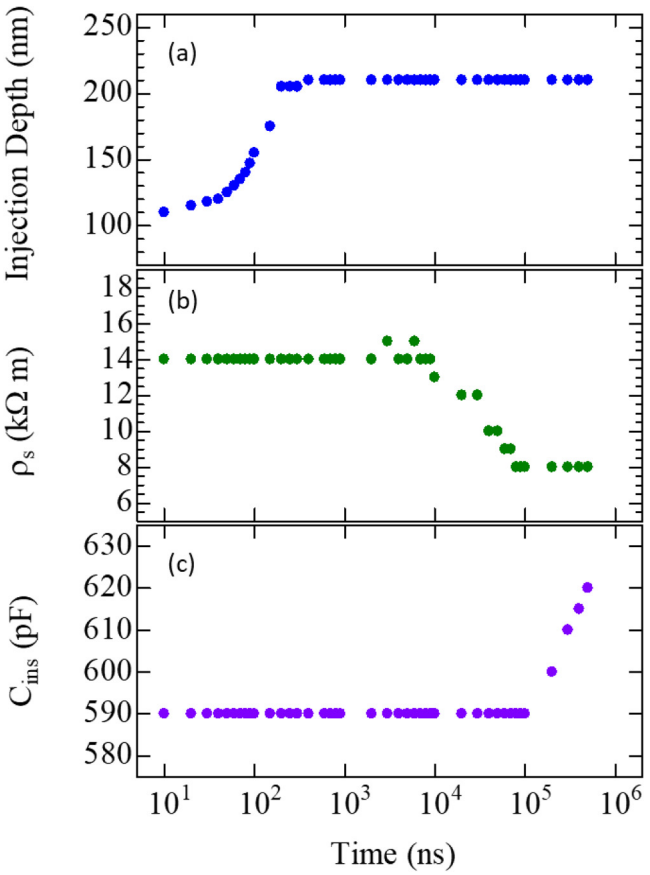

FIG. 3. Time evolutions of elemental circuit parameters: (a) hole injection depth, x, (b) electrical resistivity of hole-injected region, ρ_s, and (c) capacitance of insulator, C_{ins}.

from both rising and falling edges were consistently well fitted throughout. The main variables used in fitting the falling-edge waveforms are carrier-injection depth x, resistivity of the carrier-injected region ρ_s, and capacitance of the gate insulator C_{ins}. The carrier-injection depth x increases as the carriers are injected into the vertical thickness direction (Fig. 3). The resistivity ρ_s decreases with increasing density of injected carriers in the carrier-injected region. The time variation of C_{ins} reflects the increase in area of the injected-hole-distributed region along the semiconductor/gate insulator interface. We focus here on pre-channel formation occurring after vertical carrier-injection and before the appearance of the in-plane diffusion of holes.

The time variations of x, ρ_s, and C_{ins} (Fig. 3) describe the temporal evolution of the carrier-injection. The horizontal axis of this figure is logarithmic scale of elapsed time to overlook the wide time range of the carrier dynamics from 10^1 to 10^6 ns. The hole injection depth x increases from an initial penetration depth of approximately 110 nm to a depth equal to the thickness of the semiconductor layer of 210 nm in 200 ns. The initial penetration depth is the lowest observed value of x, the depth depends on the physical parameters of the semiconductor/metal junction. From Fig. 1, the holes initially penetrate into the pentacene/Au contact even at 0 V. The corresponding initial penetration depth was also estimated to be about 110 nm. During penetration by the hole front line in the first 200 ns , the vertical hole mobility across the layer was estimated to be $1.2 \times 10^{-3}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. In this estimation, effect of the space charge field in this time region was considered by the feedback of the results of the device simulator which include Poisson's equation.

In contrast, the resistivity ρ_s decreased from 14 to 8 kΩ m after the injected-hole front line had reached the semiconductor/gate insulator interface, taking roughly 10^4 ns. This decrease is associated with the accumulation of excess holes in the carrier-injected region of the pentacene layer, discussed later along with the results of the device simulator. Then, C_{ins} begins to increase after 10^5 ns, after ρ_s drops to 8 kΩ m because of the excess hole accumulation. Here, we have to briefly mention that the increase of C_{ins} may seem to be linear to $\log_{10} t$, however, the realistic time dependence of the hole frontline is near $\sqrt{t}$ after the transformation from C_{ins} to displacement of hole frontline location, as have been discussed in former research works in the framework of carrier diffusion.[1–18] However, the details of time dependence of the hole diffusion will be discussed in our next paper because the main subject in this paper is pre-channel formation process as explicitly expressed in the title. In our previous work,[19] we focused on the initial vertical carrier-injection toward the thickness direction. In this paper, we discuss the pre-channel

formation process after the vertical carrier-injection. The channel spreading is after the pre-channel formation, therefore, we would like to discuss the hole spreading in our next paper.

A point of note is the time lag between 200 ns and 10^5 ns. Within 200 ns, the front line of injected holes has already reached the semiconductor/gate insulator interface. However, the beginning of lateral diffusion of holes starts roughly from 10^5 ns and before that, an decrease in ρ_s is observed. These were significant but mysterious and cannot be understood within the equivalent circuit model. The entire spatial distribution of holes and its time evolution must be comprehended at least. Therefore, we employed device simulator ADVANCE/TCAD (AdvanceSoft Corp.), a commercial and integrated package for generic device modeling and simulations. Since the discussion using the calculated results below become long, we give a short answer for the time lag in advance. The cause of the time lag is that the finite time (CR time constant) is necessary to charge C_{ins} through vertical R, including R_c and R_s in Fig. 5(e).

Temporal snapshots of the calculated hole distribution were simulated with the device simulator (Fig. 4). This calculation was performed employing a realistic sizeable modeling of the poly-Si TFT structure but replacing the material parameter values of poly-Si with known values of pentacene[55–60] as this simulator is not implemented to consider organic semiconductors at present. Because our device is not very crystalline, we recognized that our sample was closer to an isotropic semiconductor layer. The device simulation was run on a Linux computer with a Core i7 processor in multicore parallel calculation using a message passing interface (MPI) with a 64 GB memory. The three-dimensional real-scale device structure was configured as follows. A semiconductor thin film of thickness 210 nm was placed on a sufficiently wide SiO_2(900 nm)/Si substrate. Therefore, the whole plane of the semiconductor/gate insulator interface functioned as a gate electrode. A square top-contact Au electrode (30 nm) was placed on the semiconductor layer [Fig. 5(a)]. The colored square seen at bottom-left in Fig. 5(a) corresponds to the projection of the contact electrode; a detailed discussion of the configuration is described later.

Holes from the contact electrode initially penetrated the semiconductor layer at 0 ns, i.e., before the application of V_{GS} [Fig. 4(a)]. Then, 40 ns after the application of the constant V_{GS} of −5 V, the front line of the calculated hole distribution descends with increasing thickness depth [Fig. 4(b)] and corresponds to an initial carrier-injection from the contact electrode into the semiconductor layer, as well as an increase in x from TDT experimental data [Fig. 3(a)]. After 500 ns, injected holes begin to accumulate in number at the semiconductor/gate insulator interface and with this increase in the channel plane, the width of the hole distribution begins to expand [Figs. 4(e) and 4(f)]. This is the lateral hole diffusion reported from many previous optical observations.[1–18] In addition, one can see a hole depletion seen in the peripheral of the channel gradually spread toward the right side of the figure. The reason for the extending a hole depletion is that the holes in the peripheral region of the channel are gradually moving toward the channel. Since a strong electric field exist in and around the capacitor structure between the gate electrode and the contact electrode, thermal equilibrium holes distributed around the channel moved toward the channel.

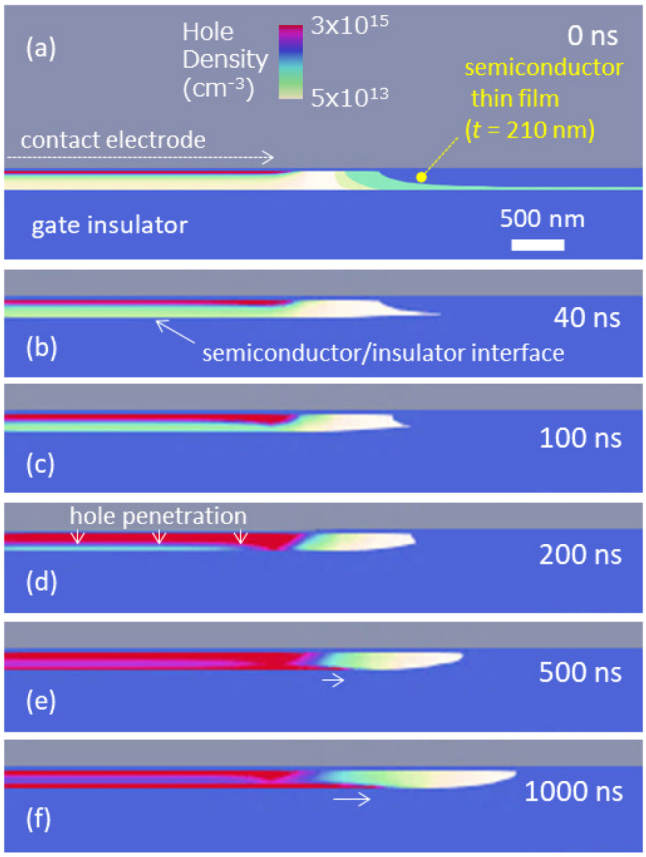

FIG. 4. Time variation of the calculated hole density in the bottom gate and the top-contact TFT structure near the source electrode at (a) 0 ns, (b) 40 ns, (c) 100 ns, (d) 200 ns, (e) 500 ns, and (f) 1000 ns. The calculations were performed with the three-dimensional ADVANCE/TCAD device simulator replacing known physical parameters of poly-Si for those of pentacene. Anisotropic carrier mobility and the presence of grain/domain boundaries and intra-domain band-edge fluctuations[76–78] are not included in this calculation.

Viewing Fig. 3 and referring to the above, we see that the hole front line reaches the semiconductor/gate insulator interface in 200 ns [panel (a)] and that hole diffusion begins after about 10^5 ns [panel (c)]. There is a time lag between the time the hole front line reaches the bottom of the semiconductor layer and the hole distribution begins to spread. To elucidate its cause, we investigated the hole distribution at the semiconductor/gate insulator interface and its time evolution in both experiments and calculations.

The calculated time variation of the hole distribution in the semiconductor/gate insulator interface plane [Figs. 5(a)–5(c)] show that after 500 ns, from the beginning of V_{GS} application, the region below the contact electrode [panel (a), red square region in the bottom-left corner] has a high hole concentration. In the beginning, the holes emanate from the contact electrode and accumulate below the contact electrode. After 2000 ns [panel (b)], the holes spread out toward the periphery. The driving principle underlying this expansion has been discussed and described as lateral hole

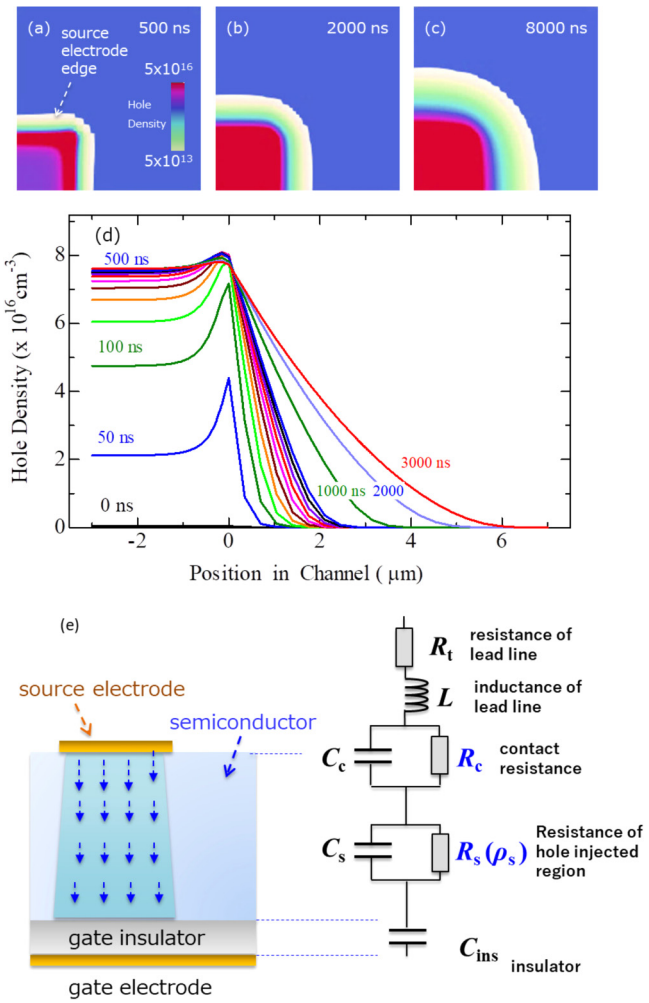

FIG. 5. (a) Calculated hole distribution in semiconductor/gate insulator interface plane at 500 ns. A square seen in the bottom-left corresponds to the projection of the contact electrode. (b) and (c) are taken at 2000 and 8000 ns, respectively. (d) Profiles of the calculated hole density in the semiconductor/gate insulator interface plane taken at different times from 0 to 3000 ns. The horizontal axis is the distance along the channel; the origin corresponds to the point directly below the contact electrode edge. (e) Schematic of a hole-injected TFT and corresponding equivalent circuit at this stage.

diffusion.[1–18] As already mentioned, the main issue is the time lag and hence, this period of hole diffusion in this region will be addressed on another occasion.

Figure 5(d) gives the hole profile along the x-direction in the channel plane [panels (a)–(c), the horizontal axis]. The coordinate origin is set directly below the contact electrode edge. The hole density gradually increases with increasing elapsed time up to 500 ns; however, the increase is almost confined in the area just below the contact electrode during this stage. After hole density saturates in the confined region during the initial 500 ns, in-plane hole diffusion proceeds. Therefore, in-plane hole diffusion begins after a steady state is reached in the equivalent circuit determined by C_{ins}, R_c, and R_s [panel (e)] corresponding to Fig. 2(b) of Ref. 19. With C_{ins} saturation as holes accumulate, the electric field that confines holes between the contact and gate electrodes weakens; that is, holes are collected and accumulated until the electric field in the capacitor sufficiently decreases. From the viewpoint of electrical circuit theory, a finite time is spent to charge the CR series circuit. This finite time delays the rise in TFT significantly (i.e., the frequency characteristics change for the worse). Therefore, to speed up the device, values for R_c, R_s, and C_{ins} must be reduced. R_c can be effectively decreased by inserting a carrier-injection layer or a self-assembled monolayer.[68–75] R_s can be reduced by decreasing the thickness of the semiconductor layer; indeed, molecular-layered TFTs demonstrate high performances.[61–67] Therefore, the reduction of both the contact and access resistances is crucial not only for static electrical properties but also for the dynamical response of TFTs. The reduction of C_{ins} is more a secondary factor as far as an ideally constructed conventional top-contact and bottom gate TFT is concerned. However, if all other settings including R_c and R_s are the same, a smaller C_{ins} is better for high-speed operations. In addition, apart from structural and dielectric contributions to capacitance, because a realistic C_{ins} includes a contribution to the capacitance from the hole trap site, the hole trap density should be reduced so as not to obstruct channel formation. A discussion of this effect of hole trap density will be given in a forthcoming article.

From the viewpoint of experiment based on TDT (Fig. 3), we proposed a dynamical TFT channel formation as outlined below. The front line of holes injected from the contact electrode reaches the semiconductor/gate insulator interface in 10^1–10^2 ns, the time interval depending on the vertical carrier mobility, applied electric field strength, thickness of the semiconductor layer, and contact resistance. The holes are successively injected through a series connection with a contact resistance and a resistance associated with the hole-injected semiconductor layer. The holes accumulate at the semiconductor/gate insulator interface directly below the contact electrode until the capacitance plateaus. During hole accumulation, the resistance of the hole-injected semiconductor region decreases because the hole density increases, corresponding to a decrease in ρ_s [Fig. 3(b)] in a 10^4 ns time period. After the holes are confined by a vertical strong electric field in the structural capacitor, the hole density plateaus, the excess distribution of holes diffuses outward into the lateral plane over a time period of 10^4–10^5 ns, which depends on the horizontal hole mobility, hole trap density in both bulk and at the interface, and other factors limiting hole conduction such as grain/domain boundaries and intra-domain band-edge fluctuations.[76–78] In particular, these last two factors are not included in the present device simulations at all. Differences in time intervals between the present simulation and experimental data may well be due to these factors.

IV. CONCLUSIONS

We presented an analysis of both the experimental TDT data and the results from device simulations of the pre-channel formation in a OTFT structure from the beginning of hole injection across layers to the channel formation by in-plane diffusion of

accumulated holes at the semiconductor/gate insulator interface. We focused on the time lag from when the hole front line reached the semiconductor/gate insulator interface (i.e., carrier-injection depth x plateauing) to the beginning of the in-plane spreading of the holes (i.e., capacitance C_{ins} beginning to increase) that was experimentally observed in the TDT data. During this time lag, the holes were accumulating in the semiconductor/gate insulator interface in finite time, corresponding from an equivalent electrical circuit perspective to the charging of a capacitor via a contact resistor and an access resistor.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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